IN THE SPECIFICATION:

Please replace the following paragraphs.

Page 2, Paragraph [0006]:

Prior art methods of controlling parasitic inductance include connecting an external capacitor between the supply leads. This connection creates a passive bypass that decreases the supply line oscillation due to external inductances. However, it does not significantly reduce the oscillation caused by internal inductances. Another prior art method includes connecting [[on]]an on-chip capacitor between the internal supply leads. The capacitor acts as a bypass in the same manner as an external capacitor. However, in order to be effective, the internal capacitor must be very large. This has the drawback of occupying a significant portion of the chip area. Consequently, this method is generally undesirable when minimization of the die area is of great importance.

Page 3, Paragraph [0009]:

Figure 5a shows a schematic 44 of an implementation of the method of Figure [[3]]4. The circuit shows mutually exclusive CMOS switches that configure the capacitors (C2) 46 and (C1) 48 to either be in the charging phase (shunt across Vdd/Vss) or in the discharging phase (in series with Vdd/Vss). The circuit has two sections: the V_{ave} (average voltage) tracking loop 50 and the V_{inst} (instant voltage) monitor and charge pump loop 52. The monitor and charge pump loop 52 is physically located on the chip. The switches are driven by two complementary drivers (comparators) 54 and 56. These drivers each provide two outputs with enough voltage offset to ensure minimal leakage

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through both charge and discharge switches during switching activity.

Page 4, Paragraph [0011]:

Figure 5b shows the operation of the circuit shown in Figure 5a. Specifically, the graph shows: a steady state when $V_{inst}=V_{ave}$; a discharging phase when $V_{inst}<V_{ave}$; and a charging phase when $V_{inst}[[<]] \geq V_{ave}$. The high frequency and low frequency cutoffs are also shown for their respective phases.

Page 7, Paragraph [0032]:

Figures 7a and 7b show a block diagram 75 of a model of the power distribution system of a chip in accordance with one embodiment of the present invention. Figure 7a shows the connection from the package via 72 is split into parallel paths that connect to nine separate models 76a-76i for the "bump and grid" "components of the chip. These components are generally the connections, circuit paths, etc. of the chip. Each of the bump and grid components 76a-76i is then connected by a via 78a-78i to a designated chip section model. Figure 7b shows a block diagram 79 of an inter-connecting grid of nine section models 80a-80i and ten routing channel models 82a-82l. Each section model 80a-80i is connected to other adjacent section models through the routing channel models 82a-82l. The nine sections are arranged in a three-by-three grid with the [[ten]]twelve channels serving as connections between each of the sections.

Page 8, Paragraph [0033]:

While Figures 7a and 7b show nine bump and grid models 76a-76i, nine section

models 80a-80i, and [[ten]]twelve routing channels 82a-82l, it is fully intended that the scope of this invention covers embodiments with differing numbers of each of these components. For example, the chip could be represented by a four-by-four section model grid. The end result is that different arrangements and numbers of the component blocks shown in Figures 7a and 7b are dependent upon the components present in the system and are not limited to the embodiment shown here.